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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/593,280	09/18/2006	Yukio Arima	071971-0735	7818

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EXAMINER	
RIZK, SAMIR WADIE	

ART UNIT	PAPER NUMBER
2112	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/593,280	ARIMA, YUKIO	
	Examiner	Art Unit	
	SAM RIZK	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1* is/are rejected.

7)☒ Claim(s) *2-14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 September 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/18/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTIONS

- Claims 1-14 have been submitted for examination
- Claim 1 has been rejected
- Claims 2-13 have been objected to

Specification

1. The abstract of the disclosure is objected to because it lacks the background of the invention that relates to a path memory circuit used in Viterbi decoding for storing survival path information for each state. Appropriate action is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Miyauchi et al. US publication no. 2001/0049809 (Hereinafter Miyauchi).

3. In regard to claim 1, Miyauchi teaches:

- A path memory circuit for use in a Viterbi decoding process performed based on state transitions through a number n (n is a positive integer) of states, comprising M (M is a positive integer) stages of storage circuits, each storage

circuit including n rows of selective storage circuits, each selective storage circuit including a selection circuit for selectively outputting an input according to a result of the Viterbi decoding and a storage element circuit for storing a result selectively outputted from the selection circuit, the path memory circuit comprising:

- a memory area A formed by the storage circuits of the first to ith (i is an integer from 0 to M) stages;
  (Figure 2, ref. (RAM10) in Miyauchi)
- a memory area B formed by the Selective storage circuits that select and hold a decoding result for any state k (k is an integer from 1 to n) of the storage circuits from the i+1th stage to the Mth stage; and
  (Figure 2, ref. (RAM11) in Miyauchi)
- a memory area C formed by the selective storage circuits other than the memory area A and the memory area B,
  (Figure 2, ref. (RAM12) in Miyauchi)
- wherein according to a memory length control signal, the storage circuits of the j (j is an integer from i+1 to Mth and subsequent stages in the memory area C are stopped, and the selection circuits of the jth and subsequent stages in the memory area B select an output of the selective storage circuits of a preceding storage circuit belonging to the memory area B.
  (sections [0053]-[0058] in Miyauchi)

Allowable Subject Matter

4. Claims 2-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

REASONS FOR ALLOWANCE

The following is an examiner's statement of reasons for allowance:

5. Claim 2 of the present application teaches, for example,

memory length setting means for setting, to a first state, the memory length control signal to the storage circuit of a stage so as to set a path memory length to an intended length depending on a status of a signal to be Viterbi-decoded; and logical sum means for, when the memory length control signal to the storage circuit of a stage is set to the first state, setting, to the first state, the memory length control signal to the storage circuit of the following stage.

The foregoing limitations are not found in the prior art of record. Particularly, none of the prior arts of record teach nor fairly suggest the cited limitation;

memory length setting means for setting, to a first state, the memory length control signal to the storage circuit of a stage so as to set a path memory length

to an intended length depending on a status of a signal to be Viterbi-decoded; and logical sum means for, when the memory length control signal to the storage circuit of a stage is set to the first state, setting, to the first state, the memory length control signal to the storage circuit of the following stage.

6. Claim 3 of the present application teaches, for example,

convergence determination means for, when it is determined that outputs from all the storage element circuits of a stage are equal to one another, setting, to a first state, the memory length control signal to the storage circuit of the following stage; and logical sum means for, when the memory length control signal to the storage circuit of a stage is set to the first state, setting, to the first state, the memory length control signal to the storage circuit of the following stage.

The foregoing limitations are not found in the prior art of record. Particularly, none of the prior arts of record teach nor fairly suggest the cited limitation;

convergence determination means for, when it is determined that outputs from all the storage element circuits of a stage are equal to one another, setting, to a first state, the memory length control signal to the storage circuit of the following stage; and logical sum means for, when the memory length control signal to the

storage circuit of a stage is set to the first state, setting, to the first state, the memory length control signal to the storage circuit of the following stage.

7. Claims (4-14) are allowable if claims 2 and 3 limitations are incorporated into the independent claim 1.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sam Rizk whose telephone number is (571) 272-8191. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronics Business Center (EBC) at 866-217-9197 (toll-free)

/Sam Rizk/

Examiner, Art Unit 2112